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SLATER & MATSIL LLP
17950 PRESTON ROAD
SUITE 1000
DALLAS, TX 75252

EXAMINER	
TRAN, BINH X	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/721,225	LUETZEN ET AL.	
	Examiner	Art Unit	
	Binh X. Tran	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 21-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 21-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submissions filed on August 29, 2008 and September 19, 2008 have been entered.

Response to Amendment

2. The affidavit filed on August 29, 2008 under 37 CFR 1.131 is sufficient to overcome the Kudelka (US 6,566,273) reference.

3. Applicant's arguments, see page 12, filed August 29, 2008, with respect to the certified copy of an English language translation of the priority document have been fully considered together with the submission on September 19, 2008 and are persuasive. The rejection under 35 U.S.C. 102 being anticipated by Kudelka (US 6,566,273) has been withdrawn.

Drawings

4. The drawings are objected to because the graph in figure 8 is labeled in German. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version

of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

Claim Objections

5. Claims 1, 21, 22, 28, 30, and 41 are objected to because of the following informalities:

In Claims 1, 21, and 28, the wording of the claims makes it unclear as to whether the defining of the grid on the surface of the substrate and the selection of areas within the grid can be accomplished simultaneously. The specification suggests that both the defining of the grid and the selection of grid rectangles can occur simultaneously. In paragraph 0052 in the specification, the structure of the substrate is described with reference to a grid. However, no grid is defined in the preferred embodiment in paragraph 0059 except using a mark to align a mask with openings that select areas.

Thus, in the preferred embodiment, the defining and the selection steps occur simultaneously. The examiner interprets the claims so that the defining of the grid and the selection of the areas can occur simultaneously. In line with the specification, the alignment of a mask with the proper openings is sufficient to both define the grid and select areas within the grid.

In Claim 1, "sidewalls formed in a depth under the surface of a semiconductor substrate" could simply mean that an etched pattern has a bottom lower in depth as compared to the surface of the substrate and that sidewalls surround the bottom. Alternatively, the term could mean that the etched patterns extend some distance non-vertically underneath the etched hole on the surface. The examiner suggests that this phrase be reworded.

6. In Claims 21 and 28, it is unclear whether applicants mean to introduce an additional limitation by the use of the term “checker-board fashion." The grid on a checker board has grid rectangles that are all roughly equal in size and are squares. The examiner suggests that the nature of the phrase be more clearly indicated.

7. In Claims 22 and 30, the examiner suggests a rewording of the phrase "the semiconductor substrate by means of an exposure device with the x, y axes of the surface grid parallel to the crystal faces” to clarify that the x, y axes are on the substrate and not on the exposure device. For the purposes of this rejection, the grid will be interpreted as being defined on the substrate rather than the exposure device.

8. In Claim 41, "the lower portions of the trenches structures extend beneath the secondary structure” should be modified. First, the examiner suggests that “trenches"

should be replaced with “trench’s” or "trenches’." Second, the examiner suggests that the claim should be limited to trenches with lower sidewalls that extend non-vertically beneath the secondary structures. As written, the claim limitation includes any trench in which the bottom of the trench extends lower as compared to the surface of the substrate than the bottom of the access transistor does.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

10. Claim 23 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "large structure" in claim 23 is a relative term which renders the claim indefinite. The term "large structure" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. In addition, the structure referred to in the phrase "the large structure" in claim 23 is unclear because of lack of antecedent basis.

Claim 23 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 23 recites the limitation "a layout of the large structure" in the first sentence. There is insufficient antecedent basis for this limitation in the claim. "The large structure" is not defined and could refer to the semiconductor substrate or to the entire mask including the edges of the mask. The examiner suggests that the phrase "a layout of the large structure" be deleted.

11. Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are:

In Claim 21, the definition of area in the phrase “area selective etching” is unclear. "Area selective etching" for increasing the size of the trench structures in a depth under the semiconductor surface could mean etching that is area selective in that it selects certain trenches and increase the width of those trenches some depth below the surface of the substrate without regard to whether the surface openings are simultaneously widened. The result could be two different types of trenches, one uniformly wider at all depths than the other. Or, the terms could also mean the use of etching to selective expand every trench. The expansion is such that the surface opening maintains its original shape with negligible expansion in its dimensions. For the purposes of the section 103 rejection, the term “area selective etching” will be given the second meaning.

In Claim 21, the term "secondary structure" appears without reference to any structure described as a primary structure. Secondary structures could mean the bottle etching of a structure within the trenches after the openings in the substrate surface are protected, or secondary structures could mean the components other than trench capacitors typically need for DRAM cells. The specification fails to supply a clear definition, see paragraph 0013.

12. Claim 44 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: at least the using of a method of etching because “using a marking to orient a patterned mask” does not adequate "comprise” the etching of a substrate. For the purpose of the 103 rejection below, the claim will be treated as if it said “using a marking to orient a patterned mask.”

13. Claims 2-13 are indefinite because they directly or indirectly depend on indefinite claim 21.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

15. Claims 1, 22, 23, and 27 are rejected under 35 U.S.C. 103(a) as obvious over Kudelka (US 2001/0016398) in view of Yasue (JP 05-109984).

16. With respect to claim 1, Kudelka et al. (US 2001/0016398) discloses a method of creating a trench in a monocrystalline silicon substrate. Kudelka, US 2001/0016398, paragraph 0012. This crystalline material has a crystal lattice with crystal faces that are more resistant to etching and with crystal faces that are less resistant to etching, Kudelka, US 2001/0016398, paragraph 0013. Monocrystalline silicon can also be used as a semiconductor. Kudelka, US 2001/0016398, paragraph 0012.

Kudelka discloses selecting areas and etching a surface opening within selected areas. Kudelka, US 2001/0016398, paragraph 0035. The selected areas are regularly arranged with respect to crystal orientation. Kudelka, US 2001/0016398, paragraph 0035, fig. 15, and fig. 16. Kudelka also teaches the step of etching sidewalls of the trench structures formed in a depth under the surface of the semiconductor substrate. Kudelka, US 2001/0016398, paragraph 0043. The etched pattern in Kudelka has a bottom lower than the surface level of the substrate and sidewalls surround the bottom. Kudelka, US 2001/0016398, fig. 8. Also, the etched patterns in Kudelka extends horizontally underneath the surface of the substrate. Kudelka, US 2001/0016398, fig. 8.

The process of etching these sidewalls proceeds by etching crystal faces so as to expand the sidewalls underneath the regularly arranged selected areas. Kudelka, US 2001/0016398, paragraph 0044, fig. 15, and fig. 16.

Administrative notice is taken that a person of ordinary skill in the art at the time of the invention would know that an array of rectangles that are not squares can form a rectangular grid. The steps of defining a grid and selecting areas within the grid can occur simultaneously by means of a patterned mask aligned with respect to crystal orientation, see first paragraph under the heading "Claim Objections" above. To phrase it differently, a grid can be defined on a surface by laying out some physical pattern other than a physical pattern composed of a plurality of lines with lengths substantially greater than widths that run parallel and perpendicular to each other. Thus, a patterned mask can define a grid. By means of lithographic techniques, Kudelka discloses a step of defining at the surface of the semiconductor substrate a regular arrayed mask layer which selects etching areas that would fit into rectangular surface grid. Kudelka, US 2001/0016398, paragraph 0035, fig. 15, and fig. 16. Kudelka selects areas with reference to the <110> crystal orientation. Kudelka, US 2001/0016398, fig. 15 and fig. 16.

Although Kudelka defines a grid with respect to the <110> orientation, Kudelka does not contain the step of defining a grid with respect to the <100> crystal orientation. Yasue (JP 05-109984) discloses the application of a mask oriented by a marking so that the openings of the mask align with the <100> crystal orientation of the substrate. Yasue, JP 05109984, paragraph 0051 and drawings 6 and 10. Yasue teaches the

alignment of a mask with reference to the <100> crystal orientation to make oxide films more uniform. Yasue, JP 05-100984, paragraph 0048. The holes in the mask and the resulting trenches select areas that would fit into a rectangular surface grid parallel to the <100> crystal orientation. Yasue, JP 05109984, paragraph 0051 and drawings 6 and 10. Administrative notice is taken that a person of ordinary skill in the art at the time of the invention would know that two axes created at right angles from one another with reference to a two-dimensional surface are frequently referred to in the art as one x-axis and one y-axis.

Yasue also discloses the creation of a physical rectangular surface grid on a silicon substrate. Yasue, JP 05-109984, paragraph 0038. This grid identifies the <110> crystal orientation (faces). Yasue, JP 05-109984, paragraphs 0038 and 0046. The physical creation of the grid precedes the selection of certain grid squares for etching of trenches. Yasue, JP 05109984, paragraph 0046 and drawing 6.

17. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kudelka in view of Yasue by defining a grid with respect to the <100> crystal orientation because such orientation helps make oxide films more uniform.

18. With respect to claim 22, Kudelka discloses the use of an exposure device to image a trench structure onto the surface of the semiconductor substrate. Kudelka, US 2001/0016398, paragraph 0035.

19. With respect to claim 27, Kudelka teaches etching a surface opening of the trench with oval cross section. Kudelka, US 2001/0016398, paragraph 0052 and fig. 14.

These surface openings can later be expanded. Kudelka, US 2001/0016398, paragraph 0053.

20. With respect to claim 23, Kudelka does not disclose the use of a mask having rectangular mask openings. Kudelka teaches that the use of wet etching to create rectangular portions of trenches creates a smoother surface than conventional methods of etching do. Kudelka, 2001/0016398, paragraph 0013. Administrative notice is taken that a person of ordinary skill in the art at the time of the invention would know that a square is a type of rectangle. Yasue teaches the use of a mask with rectangular openings whose sides are parallel with the <100> crystal orientation, a crystal orientation of the semiconductor substrate that is less resistant to etching. Yasue, JP 05-109984, paragraph 0051 and drawing 10. Imaging is performed after the application of the mask. Yasue, JP 05-109984, paragraph 0051. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kudelka in view of Yasue by the creation rectangular surface openings because the use of wet etching to create rectangular portions of trenches leads to smoother surfaces than result from conventional methods of etching.

21. Claims 24, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudelka and Yasue as applied to claim 1 above, and further in view of Endoh et al. (US 7,141,506 B2).

Kudelka fails to disclose the creation of a marking identifying a crystal orientation on the substrate. Endoh et al. (US 7,141,506 B2) teaches the creation of a mark to increase the accuracy of the alignment between the crystal lattice of the substrate and a

photomask. Endoh, US 7141506 B2, col. 2, line 17. Endoh discloses a process in which a semiconductor substrate, in particular a substrate composed of silicon in wafer form, is marked with reference to the crystal orientation <100>. Endoh, 7141506 B2, col. 5, line 22 and col. 6, line 46. This marking identifies a crystal orientation of the crystal lattice. Endoh, 7141506 B2, col. 10, line 28. The crystal face whose orientation is identified by the marking, crystal orientation <100>, is less resistant to etching. Endoh, 7141506 B2, col. 10, line 16. Endoh teaches that the marking can be used for orienting a photomask. Endoh, 7141506 B2, col. 6, line 50. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kudelka and Yasue in view of Endoh by creating a marking on the substrate in order to align a photomask because the creation of a mark increases the accuracy of the alignment between the crystal lattice of the substrate and the photomask.

22. Claims 2, 7, 8, 11, 12, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudelka (US 2001/0016398) in view of Sakao (US 2001/0050436).

23. The limitations of claim 2 have been discussed above under Kudelka. (Please see paragraph 18.)

24. The limitations of claim 7 have been discussed above under Kudelka. (Please see paragraph 19.)

25. With respect to claims 8 and 21, Kudelka et al. (US 2001/0016398) discloses a method of creating a trench in a monocrystalline silicon substrate. Kudelka, US 2001/0016398, paragraph 0012. This crystalline material has a crystal lattice with crystal faces that are more resistant to etching and with crystal faces that are less

resistant to etching, Kudelka, US 2001/0016398, paragraph 0013. Monocrystalline silicon can also be used as a semiconductor. Kudelka, US 2001/0016398, paragraph 0012. Kudelka discloses selecting areas and etching a surface opening within selected areas. Kudelka, US 2001/0016398, paragraph 0035. The selected areas being regularly arranged with respect to crystal orientation. Kudelka, US 2001/0016398, paragraph 0035, fig. 15, and fig. 16.

Kudelka also teaches the step of performing area-selective etching to increase the structure size of the trench in a depth under the semiconductor's surface. Kudelka, US 2001/0016398, paragraph 0043. The etched patterns in Kudelka extends horizontally underneath the surface of the substrate into areas that initially were not chosen for the creation of surface openings. Kudelka, US 2001/0016398, fig. 8. When choosing the locations for the surface openings, Kudelka chooses areas with reference to the <110> crystal orientation. Kudelka, US 2001/0016398, fig. 15 and fig. 16. The process of etching proceeds by area-selective etching part of the trench walls to form new structures, the expansion occurring along the crystal faces that are less resistant to etching. Kudelka, US 2001/0016398, paragraph 0044, paragraph 0045 and fig. 8.

Administrative notice is taken that a person of ordinary skill in the art at the time of the invention would know that two axes created at right angles from one another with reference to a two-dimensional surface are frequently referred to in the art as one x-axis and one y-axis.

However, Kudelka does not illustrate an embodiment in which locations for the creation of surface openings are chosen in a "checker-board fashion." Sakao (US

2001/0050436) teaches a compact pattern of surface openings that reduces the amount of unused space within a DRAM cell. Sakao, US 2001/0050436, paragraphs 0021 and 0022. In particular, Sakao discloses an arrangement of trench openings that shows an active selection of alternating grid rectangles in both the rows and the columns such that no two chosen areas are adjacent. Sakao, US 2001/0050436, fig. 2 and paragraph 0080. Trench structures are formed in the chosen grid rectangles at the surface of the semiconductor substrate. Sakao, US 2001/0050436, paragraph 0081. Sakao teaches that the distances between the surface openings can be equal. Sakao, US 2001/0050436, paragraph 0068.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kudelka in view of Sakao by using a compact cell layout because the layout reduces the amount of unused space with the DRAM cells.

26. With respect to claim 11, Kudelka (US 2001/0016398) provides the upper section of the trench structures (under the surface of the substrate but above a lower edge of a trench) with a protective layer that is resistant to etching. Kudelka, US 2001/0016398, paragraph 0048 and fig. 10. The protective layer resists the etching used to expand the lower portion of the trench. Kudelka, US 2001/0016398, fig. 7 and fig. 8 and paragraph 0049.

27. With respect to claim 12, Kudelka discloses that its trenches are designed so that they may be used as storage capacitors. Kudelka, US 2001/0016398, paragraph 0033.

28. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kudelka and Sakao as applied to claims 2 and 21 above, and further in view of Yasue (JP 05-109984).

The limitations of claim 3 have been discussed above under Kudelka and Yasue. (Please see paragraph 20.)

29. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudelka and Sakao as applied to claims 8 and 21 above, and further in view of Yasue (JP 05-109984).

Kudelka discloses that the <100> crystal faces are less resistant to etching than the <110> crystal faces. Kudelka, US 2001/0016398, paragraph 0044.

Kudelka fails to teach a surface grid oriented in accordance with a <100> crystal orientation. The steps of defining a grid and selecting areas within the grid can occur simultaneously by means of a patterned mask aligned with respect to crystal orientation, see first paragraph under the heading “Claim Objections” above. Yasue teaches the alignment of a mask with the <100> crystal orientation to make oxide films more uniform. Yasue, JP 05-109984, paragraph 0048. In Yasue, the openings of the mask align with the <100> crystal orientation of the substrate. Yasue, JP 05-109984, drawings 6 and 10. Yasue teaches the creation holes in the mask and the resulting trenches would fit into a rectangular surface grid parallel to the <100> crystal orientation. Yasue, JP 05-109984, paragraph 0046 and drawings 6 and 10. Thus, Yasue teaches the creation of the grid for etching of trenches. Yasue, JP 05-109984, paragraph 0046 and drawing 6.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kudelka and Sakao in view of Yasue by defining a grid with respect to the <100> crystal orientation because such orientation helps make oxide films more uniform.

30. Claims 4, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudelka and Sakao as applied to claim 21 above, and further in view of Endoh et al. (US 7,141,506 B2).

The limitations of claims 4, 5, and 6 have been discussed above under Kudelka and Endoh. (Please see paragraph 21.)

31. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kudelka and Sakao as applied to claims 12 and 21 above, and further in view of Förster et al. (US 6,455,369).

Unlike the current claims, Kudelka does not teach the use of selection transistors. Förster et al. (US 6,455,369) teaches trench capacitors with planar selection transistors to better use the third dimension and to enable the creation of smaller capacitors. Förster, US 6455369, col. 1, lines 22 and 34. Förster discloses the creation of multiple trenches. Förster, US 6455369, col. 10, line 63 and fig. 2A-2P. Selection transistors are formed on the surface of the substrate near a trench for use with the storage capacitances of the DRAM cells. Förster, US 6455369, col. 7, line 43 and fig. 7.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kudelka and Sakao in view of Förster by using planar

selection transistors with the trenches because trench capacitors with planar selection transistors make better use of the third dimension.

32. Claims 28 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudelka (US 2001/0016398) in view of Sakao (US 2001/0050436).

With respect to claim 28, Kudelka et al. (US 2001/0016398) discloses a method of creating a trench in a monocrystalline silicon substrate. Kudelka, US 2001/0016398, paragraph 0012. This crystalline material has a crystal lattice with crystal faces that are more resistant to etching and with crystal faces that are less resistant to etching, Kudelka, US 2001/0016398, paragraph 0013. Monocrystalline silicon can also be used as a semiconductor. Kudelka, US 2001/0016398, paragraph 0012. Kudelka discloses selecting areas and etching a surface opening within selected areas. Kudelka, US 2001/0016398, paragraph 0035. The selected areas being regularly arranged with respect to crystal orientation. Kudelka, US 2001/0016398, paragraph 0035, fig. 15, and fig. 16. When selecting the locations for the surface openings, Kudelka selects areas with reference to the <110> crystal orientation. Kudelka, US 2001/0016398, fig. 15 and fig. 16. Kudelka discloses a structure that contains spaces that allow the placement of components near the surface of the substrate. Kudelka, US 2001/0016398, fig. 14 and fig. 16.

Administrative notice is taken that a person of ordinary skill in the art at the time of the invention would know that two axes created at right angles from one another with reference to a two-dimensional surface are frequently referred to in the art as one x-axis and one y-axis.

However, Kudelka does not illustrate an embodiment in which locations for the creation of surface openings are chosen in a "checker-board fashion." Sakao (US 2001/0050436) teaches a compact pattern of surface openings that reduces the amount of unused space within a DRAM cell. Sakao, US 2001/0050436, paragraphs 0021 and 0022. In particular, Sakao discloses an arrangement of trench openings that shows an active selection of alternating grid rectangles in both the rows and the columns such that no two chosen areas are adjacent. Sakao, US 2001/0050436, fig. 2 and paragraph 0080. Trench structures are formed in the chosen grid rectangles at the surface of the semiconductor substrate. Sakao, US 2001/0050436, paragraph 0081. Sakao teaches that the distances between the surface openings can be equal. Sakao, US 2001/0050436, paragraph 0068.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kudelka in view of Sakao by using a compact cell layout because the layout reduces the amount of unused space with the DRAM cells.

With respect to claim 35, Kudelka teaches etching a surface opening of the trench with oval cross section. Kudelka, US 2001/0016398, paragraph 0052 and fig. 14.

33. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kudelka and Sakao as applied to claim 28 above, and further in view of Förster et al. (US 6,455,369).

The limitations of claim 29 have been discussed above under Kudelka and Förster. (Please see paragraph 31.)

34. Claims 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudelka and Sakao as applied to claim 28 above, and further in view of Yasue (JP 05-109984).

35. The limitations of claim 31 have been discussed above under Kudelka and Yasue. (Please see paragraph 20.)

36. With respect to claim 30, Kudelka discloses the use of an exposure device to image a trench structure onto the surface of the semiconductor substrate. Kudelka, US 2001/0016398, paragraph 0035.

Kudelka discloses that the <100> crystal faces are less resistant to etching than the <110> crystal faces. Kudelka, US 2001/0016398, paragraph 0044. The steps of defining a grid and selecting areas within the grid can occur simultaneously by means of a patterned mask aligned with respect to crystal orientation, see first paragraph under the heading “Claim Objections” above.

Although Kudelka defines a grid with respect to the <110> orientation, Kudelka does not contain the step of defining a grid with respect to the <100> crystal orientation. Yasue (JP 05-109984) discloses the application of a mask oriented by a marking so that the openings of the mask align with the <100> crystal orientation of the substrate. Yasue, JP 05109984, paragraph 0051 and drawings 6 and 10. Yasue teaches the alignment of a mask with reference to the <100> crystal orientation to make oxide films more uniform. Yasue, JP 05-100984, paragraph 0048. The holes in the mask and the resulting trenches select areas that would fit into a rectangular surface grid parallel to

the <100> crystal orientation. Yasue, JP 05109984, paragraph 0051 and drawings 6 and 10.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kudelka and Sakao in view of Yasue by defining a grid with respect to the <100> crystal orientation because such orientation helps make oxide films more uniform.

37. Claims 32, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudelka and Sakao as applied to claim 28 above, and further in view of Endoh et al. (US 7141506 B2).

The limitations of claims 32, 33 and 34 have been discussed above under Kudelka and Endoh. (Please see paragraph 21.)

38. Claims 36, 37, 38, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudelka et al. (US 2001/0016398) in view of Wang et al. (US 6,703,273).

With respect to claim 36, Kudelka et al. (US 2001/0016398) discloses a method of creating a trench in a monocrystalline silicon substrate. Kudelka, US 2001/0016398, paragraph 0012. The silicon substrate has <100> crystal faces and <110> crystal faces. Kudelka, US 2001/0016398, paragraph 0054. Kudelka discloses selecting areas and etching a surface opening within selected areas. Kudelka, US 2001/0016398, paragraph 0035. The selected areas being regularly arranged with respect to crystal orientation. Kudelka, US 2001/0016398, paragraph 0035, fig. 15, and fig. 16. Kudelka discloses a method of etching the substrate to form upper portions of the trench

structures, forming a protective layer over the upper portions of the trench structures, and etching the semiconductor substrate to form lower portions of the trench structures beneath and wider than the upper portions. Kudelka, US 2001/0016398, paragraph 0012.

However, Kudelka does not disclose rows and columns being parallel to <100> crystal faces. Wang et al. (US 6,703,273) discloses trench capacitors with compact rows and columns that minimize the size of the DRAM cells. Wang, US 6703273, col. 5, line 66. Administrative notice is taken that a person of ordinary skill in the art at the time of the invention would know that for monocrystalline silicon with a <100> crystal orientation, a <100> plane runs diagonally at a 45 degree angle across the substrate. See, e.g., Trah, US 5282926, fig. 1a; Endoh, US 7141506, figs. 14(b) and 15(a). Memory devices that are composed of DRAM cells frequently place the trench capacitors in rows and columns. Wang teaches trench capacitors on a monocrystalline substrate with a <100> crystal orientation. Wang, US6703273, col. 3, line 14.

Figure 1A in Wang shows rows and columns parallel to the <100> crystal faces. Wang, US 6703273, fig. 1A. Supposing that the drawing currently shows rows and columns parallel to the <110> crystal orientation, rotating the substrate by 45 degrees will create rows and columns parallel to the <100> crystal orientation because of the <100> planes running diagonally across the substrate. This is true because holes in the substrate are in a formation such that that lines connecting the centers of the holes form squares and because the holes in the substrate are small relative to the distance between them.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Kudelka in view of Wang by creating compact rows and columns of DRAM cells because a compact pattern helps minimize the size of the DRAM cells.

39. With respect to claim 37, Kudelka (US 2001/0016398) teaches etching a surface opening of the trench with oval cross section. Kudelka, US 2001/0016398, paragraph 0052 and fig. 14.

40. With respect to claim 38, Kudelka discloses trenches whose lower portions have substantially rectangular shape with sides parallel to the <110> crystal face. Kudelka, US 2001/016398, paragraph 0013 and fig. 16.

41. With respect to claim 39, Kudelka discloses that its trenches are designed so that they may be used as storage capacitors. Kudelka, US 2001/0016398, paragraph 0033.

42. Claims 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudelka and Wang as applied to claim 36 above, and further in view of Forbes et al. (US 5,907,170).

Kudelka does not disclose the creation of a plurality of capacitors with access transistors. Forbes et al. (US 5,907,170) discloses the use of capacitors with access transistors to create a realizable memory cell that uses less surface area. Forbes, US 5907170, col. 2, line 53. Forbes discloses a method of creating a plurality of capacitors in rows and columns on a monocrystalline substrate. Forbes, US 5907170, col. 6, line 19 and fig. 3. Each capacitor is associated with a trench structure. Forbes, US 5907170, fig. 3. The capacitors use access transistors that are functionally

coupled to one of the capacitors. Forbes, US 5907170, col. 2, line 57. Forbes discloses that a capacitor plate was formed in the lower portions of the trench structure, the plate being beneath the access transistors. Forbes, US 5907170, col. 6, line 42; col. 8, line 57; and fig. 3.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Kudelka and Wang in view of Forbes by creating capacitors with access transistors because such capacitors use less surface area.

43. Claims 42, 43, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudelka and Wang as applied to claim 36 above, and further in view of Endoh et al. (US 7,141,506 B2).

The limitations of claims 42, 43 and 44 have been discussed above under Kudelka and Endoh. (Please see paragraph 21.)

Response to Arguments

Applicant's arguments with respect to claims 1-13, 21-44 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh X. Tran whose telephone number is (571)272-1469. The examiner can normally be reached on Monday-Thursday and every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Binh X Tran
Primary Examiner
Art Unit 1792

/Binh X Tran/
Primary Examiner, Art Unit 1792